



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,937	09/06/2000	Jong Sang Baek	8733.289.00	8624

30827 7590 10/22/2003

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER

NELSON, ALECIA DIANE

ART UNIT	PAPER NUMBER
----------	--------------

2675

DATE MAILED: 10/22/2003

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/655,937

Applicant(s)

BAEK ET AL.

Examiner

Alecia D. Nelson

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. ***Claims 1, 2, 4, 6, 8, 9, 11, 20, and 21*** are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836).

With reference to **claims 1, 8, and 20**, Shin teaches a liquid crystal display device (100), comprising a line memory (230) for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit (270) including n driver integrated circuits (240, 250) that are connected to the line memory (230) and the liquid crystal display panel (100) to drive the liquid crystal display panel in response to the data outputted from the line memory (230); and a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every

Art Unit: 2675

period of the data clock in response to a time corresponding to the number of said groups (see column 5, line 18-column 6, line 18). With further reference to **claims 8 and 20**, Shin teaches, with reference to the summary of the invention, generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62).

With reference to **claims 2 and 9**, Shin teaches, with reference to FIG. 4, a first group (A) and a second group (B), wherein the data driver ICs are divided also into the two groups (A, B) and the video data are sent to and latched at the two groups (see col. 2, lines 43-54).

With reference to **claims 4, 6, and 11**, Shin teaches, with reference to FIG 5, that the data driver ICs are divided into two groups. One group, an odd data driver IC group (32), is the driver for ICs connected with the odd numbered data lines. The other group, an even data driver IC group (33), is for the driver ICs connected to the even numbered data lines (see column 2, lines 56-64).

With reference to **claim 21**, Shin teaches that the data storage step includes sequentially receiving at least two pixel data (odd, even) to divide and store the data for one line into two groups; the frequency division ration at the data clock generating step is two; and the two groups at the data storage step individually output the two pixel data at a desired time difference during one period of the second data clock (see column 5, line 59-coulumn 6, line 18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. ***Claims 3, 5, 7, 10, and 12*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin, as applied to **claim 1** above, and further in view of Nakano et al. (U.S. Patent 6,229,513).

Shin fails to specifically teach that the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock,

thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

Nakano et al. teaches that a clock signal (CK) is transmitted from the computer side and is divided by a D-type flip-flop (111) such that clock signals (D4, D5) are outputted from a non-inverting output terminal, and an inverting output terminal of the flip-flop (111), respectively. Also originally ordered display data transmitted from the computer side are inputted to a first, or second, memory (112, 113). The memory stores display data of an amount corresponding to a total number of drain signal lines connected to two drain drivers. The originally ordered display data transmitted from the computer side are first written into the first memory (112). When $2n$ display data are stored in the first memory (112), next $2n$ data transmitted are written into the second memory (113), and meanwhile the display data are read from the first memory (112) and outputted to the drain drivers (130) (see column 6, line 64-column 7, line 42).

6. **Claims 13-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. in view of applicant's admittance of prior art.

With reference to **claims 13, 15-19**, Nakano et al. teaches a liquid crystal apparatus having a display control means for generating control signals including at least clock signals based on input display control signals inputted thereto and sending the control signals to the driving means (see abstract). The liquid crystal display apparatus comprises a first and second memory (112, 113) for receiving and storing originally ordered display data transmitted from the computer side. The data is then

Art Unit: 2675

outputted to the drain drivers (130) through the display data bus line (134) (see column 7, lines 3-17). Drivers (130) including a group A (odd numbered) and a group B (even numbered) are connected between the liquid crystal panel (10) and the memory (112, 113) comprised in the display control unit (110) (see column 6, lines 16-37). Within the display control unit (110) a clock signal (CK) is transmitted from the computer side, and is divided by a D-type flip-flop (11) such that clock signals (D4, D5) are half the frequency of the original clock signal (CK). It is also taught that the generated clock signal (D4) is used for latching display data, and the second clock signal (D5) has the same frequency as and a different phase from the first clock signal (D4), which means that clock signal (D5) is an inverted version of clock signal (D4) (see column 6, lines 24-31).

Nakano et al. fails to specifically teach that the memory receives two-pixel data unit, or that the driving circuit includes n driver integrated circuits. Nakano et al. does however teach that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130). Further, with reference to a second embodiment, a liquid crystal display of higher resolution has two bus lines (134a, b) as display data bus lines, and drain drivers (130') are connected thereto (see column 7, lines 43-50).

Moreover, and with reference to **claims 14**, applicant's admittance of prior art teaches a conventional four-port data transmission method wherein n driver IC's are connected to the liquid crystal display panel are two-division driven into left and right groups (see page 4, line 18-page 5, line 5).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the four-port driving method as taught by the applicant's admittance of prior art with the system as taught by Nakano et al. which suggest such driving technique in order to provide a liquid crystal display panel in which the video data of two data lines can be driven simultaneously, thereby improving the display quality of the liquid crystal display.

Response to Arguments

7. Applicant's arguments filed 1/10/03 have been fully considered but they are not persuasive. With reference to the applicant's arguments of the applied rejection to independent **claims 1, 8, and 20**, the examiner agrees with the applicant's statement that Shin fails to teach a timing controller for receiving a clock signal CK2 from the exterior thereof from the clock generator (200). However, Shin does teach that the timing controller receives a clock signal CK1 from the exterior thereof, and generates a second clock signal CK2, which is outputted from the timing controller. Further applicant argues that Shin does not disclose a timing controller outputting data every period of the received data clock. The second clock signal CK2 is generated from the received data clock CK1, and data is output from the plurality of groups of the line memory (230) to the driving circuit every period of the data clock signal CK2 (see figure 8). Further with reference to the disclosed invention the source sampling clocks SSC1 and SSC2 are generated from the data DCLK received by the timing controller from an

Art Unit: 2675

exterior thereof. Therefore the teachings of Shin are very similar to that of the disclosed invention. With reference to the applicant's arguments of the applied rejection to independent **claims 13 and 18**, that there is no reason to combine the teachings of the applied art to arrive at the claimed invention. However Nakano et al. teaches all that is required by the claim except, that the memory receives two-pixel data unit, or that the driving circuit includes n driver integrated circuits, but teaches with reference to a different embodiment that the first and second memories (112, 113) stores display data of an amount corresponding to a total number ($2n$) of the drain signal lines (D) connected to two drain drivers (130). Therefore there is a suggestion that it is possible for the memory to receive two pixel data units from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups, since it is possible for the memories to store display data of an amount corresponding to the total number of the drain signal lines, in order to increase the resolution of the driven display, which is also the reason as given by the applicant's teaching of related prior art. Further, applicant briefly states that the teachings of the related prior art did not cure the deficiencies of Nakano et al., but fail to go into detail as to why. Therefore the rejection as applied to the claims will be maintained.

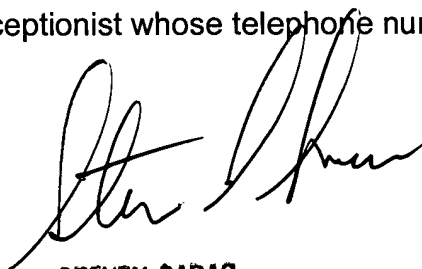
Art Unit: 2675

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.



STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

adn/ADN
October 20, 2003